OS-TR0001-FSK

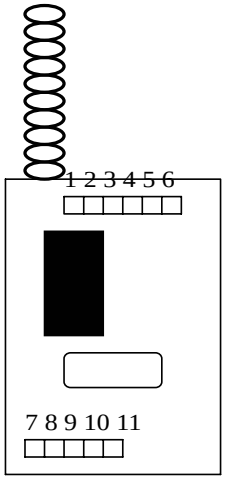
FSK TRANSCEIVER MODULE

434 MHz FSK Transceiver

Description

OS-TR0001 is an FSK Transceiver module. The OS-TR0001 is a true single-chip UHF transceiver, It base on 3 wire digital serial interface and an entire Phase-Locked Loop (PLL) for precise local oscillator generation .so the frequency could be setting. It can use in UART / NRZ / Manchester encoding / decoding. OS-TR0001 had a high performance and low cost. It could easily to design your product.

It can be used on wireless security system or specific remote-control function and others wireless system



Features

- Low power consumption.
- Integrated bit synchronizer.
- Integrated IF and data filters.
- High sensitivity (type -108dBm at 1.2kbps)
- Programmable output power -20dBm~9dBm
- Operation temperature range : -40℃～＋85℃
- Operation voltage: 2.2~3.6 Volts.
- Available frequency at : 423~443 MHz

Applications

- Car security system
- Remote keyless entry
- Garage door controller
- Home security
- Wireless mouse
- Automation system

Pin1: GND
Pin2: PALE
Pin3: PDATA
Pin4: PCLK
Pin5: DCLK
Pin6: DIO
Pin7: VCC
Pin8: VCC
Pin9: GND
Pin10:GND
Pin11:GND

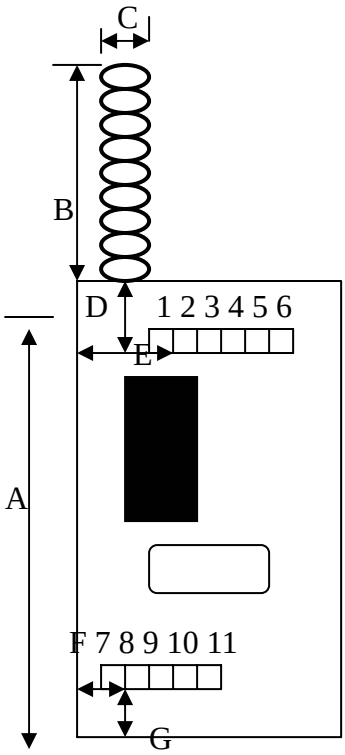
Absolute Maximum Ratings

Parameter	Rating	Units
Supply Voltage	3.6	V DC
Operating Temperature	-40 to +85	℃

Electronical Characteristics (Vcc=3V)

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typical	Max.	
Operation Voltage			2.2	3	3.6	V
Sensitivity	Psens	1.2Kbps Data Rate 434MHz		-108		dBm
Output Power	Po	Programmable	-20		10	dBm
Supply current	Icc1	TX (-20~10dBm)	5.3		28	mA
Supply current	Icc2	Receiver Mode		8		mA
Standby current	Is	Power down mode		0.2	1	uA
Crystal start-up time				3		ms
Pll lock time	Pt	Rx /Tx turn time		200		us
Pll turn on	Pn	Crystal on in power down mode		250		us
logic HIGH	VOH	Iload = 10 μ A	0.7*Vcc			V DC
logic LOW	VOL	Iload = 10 μ A			0.3*vcc	V DC
DIO setup time		Minimum time before DCLK	20			ns
DIO Hold time		Minimum time after DCLK	10			ns
Data Rate			0.6	-	76	kbps

Pin Dimension



A	34.5mm	D	3.9mm	G	3.2mm
B	20mm	E	7.1mm	Pin to pin	1.27mm
C	4.55mm	F	1.38mm		

Configuration Overview

TR1000 can be configured to achieve the best performance for different applications. Through the programmable configuration registers the following key parameters can be programmed:

- Receive / transmit mode
- RF output power
- Frequency synthesiser key parameters: RF output frequency, FSK frequency separation (deviation), crystal oscillator reference frequency
- Power-down / power-up mode
- Crystal oscillator power-up / power down
- Data rate and data format (NRZ, Manchester coded or UART interface)
- Synthesiser lock indicator mode
- Optional RSSI or external IF

Configuration Software

[redacted] provides users of **TR1000** with a software program, SmartRF® Studio (Windows interface) that generates all necessary **TR1000** configuration data based on the user's selections of various parameters. These hexadecimal numbers will then be the necessary input to the microcontroller for the configuration of **TR1000**. In addition the program will provide the user with the component values needed for the input/output matching circuit and the VCO inductor.

Figure 3 shows the user interface of the **TR1000** configuration software.

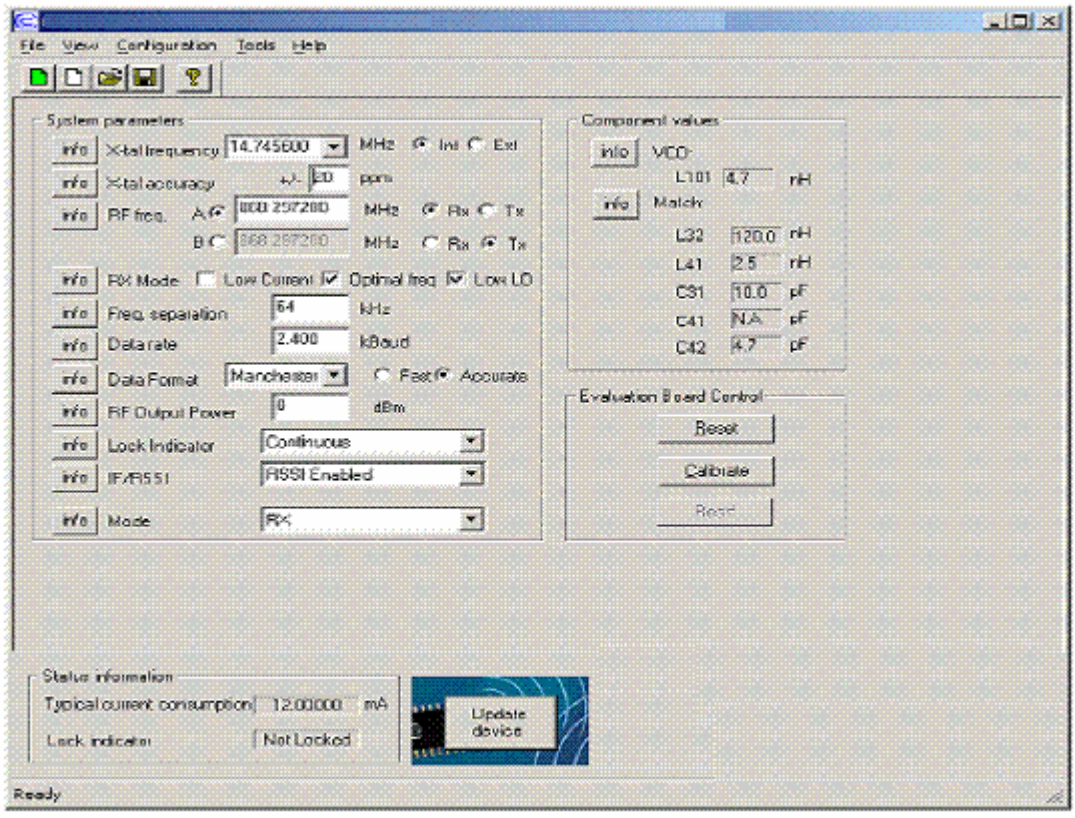


Figure 3. SmartRF® Studio user interface

3-wire Serial Configuration Interface

TR1000 is configured via a simple 3-wire interface (PDATA, PCLK and PALE). There are 28 8-bit configuration registers, each addressed by a 7-bit address. A Read/Write bit initiates a read or write operation. A full configuration of **TR1000** requires sending 22 data frames of 16 bits each (7 address bits, R/W bit and 8 data bits). The time needed for a full configuration depend on the PCLK frequency. With a PCLK frequency of 10 MHz the full configuration is done in less than 46 µs. Setting the device in power down mode requires sending one frame only and will in this case take less than 2 µs. All registers are also readable.

In each write-cycle 16 bits are sent on the PDATA-line. The seven most significant bits of each data frame (*A6:0)* are the address-bits. *A6* is the MSB (Most Significant Bit) of the address and is sent as the first bit. The next bit is the R/W bit (high for write, low for read). During address and R/W bit transfer the PALE (Program Address Latch Enable) must be kept low. The 8 data-bits are then transferred (*D7:0*). See Figure 4.

The timing for the programming is also shown in Figure 4 with reference to Table 2. The clocking of the data on PDATA is done on the negative edge of PCLK. When the last bit, *D0*, of the 8 data-bits has been loaded, the data word is loaded in the internal configuration register.

The configuration data is stored in internal RAM. The data is retained during power-down mode, but not when the power-supply is turned off. The registers can be programmed in any order.

The configuration registers can also be read by the microcontroller via the same configuration interface. The seven address bits are sent first, then the R/W bit set low to initiate the data read-back. **TR1000** then returns the data from the addressed register. PDATA is in this case used as an output and must be tri-stated (or set high n the case of an open collector pin) by the microcontroller during the data read-back (D7:0). The read operation is illustrated in Figure 5.

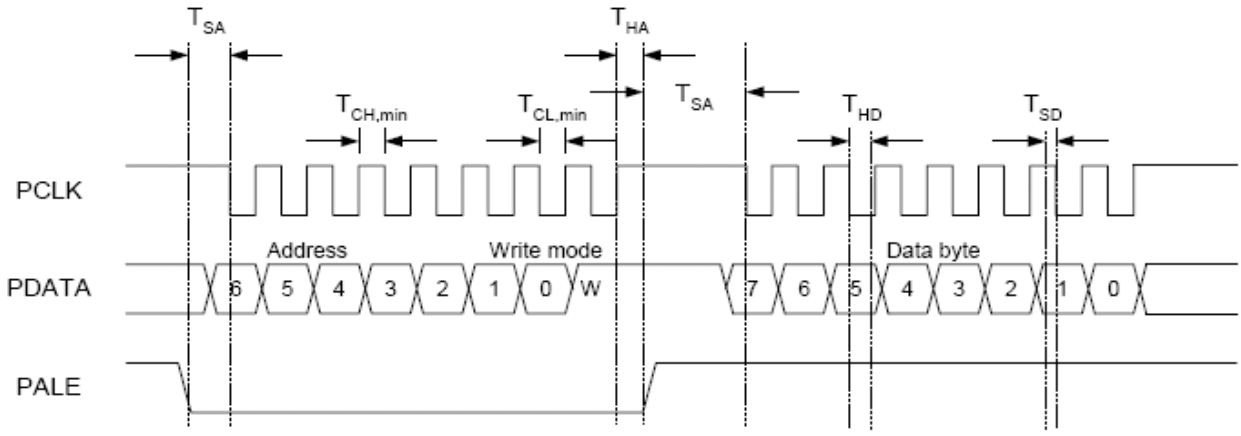
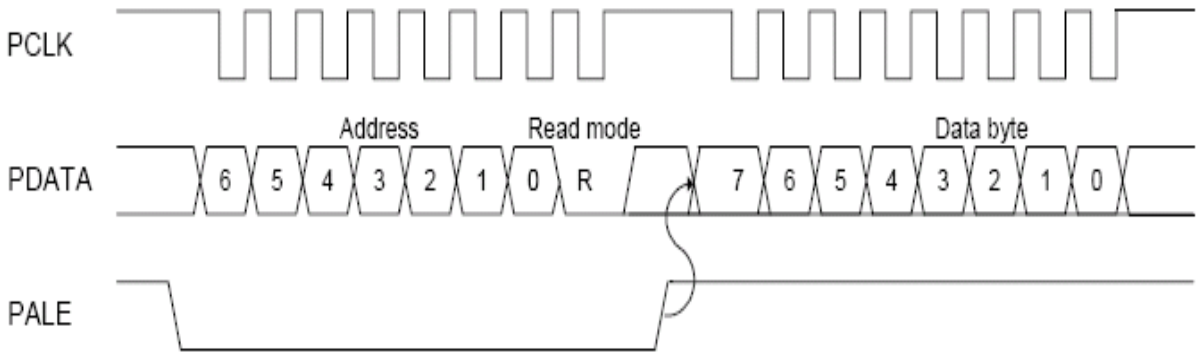


Figure 4. Configuration registers write operation



Parameter	Symbol	Min	Max	Units	Conditions
PCLK, clock frequency	F_{CLOCK}	-	10	MHz	
PCLK low pulse duration	$T_{CL,min}$	50		ns	The minimum time PCLK must be low.
PCLK high pulse duration	$T_{CH,min}$	50		ns	The minimum time PCLK must be high.
PALE setup time	T_{SA}	10	-	ns	The minimum time PALE must be low before negative edge of PCLK.
PALE hold time	T_{HA}	10	-	ns	The minimum time PALE must be held low after the *positive* edge of PCLK.
PDATA setup time	T_{SD}	10	-	ns	The minimum time data on PDATA must be ready before the negative edge of PCLK.
PDATA hold time	T_{HD}	10	-	ns	The minimum time data must be held at PDATA, after the negative edge of PCLK.
Rise time	T_{rise}		100	ns	The maximum rise time for PCLK and PALE
Fall time	T_{fall}		100	ns	The maximum fall time for PCLK and PALE

Note: The set-up- and hold-times refer to 50% of VDD.

Table 2. Serial interface, timing specification

Microcontroller Interface

Used in a typical system, **TR1000** will interface to a microcontroller. This microcontroller must be able to:

- Program **TR1000** into different modes via the 3-wire serial configuration interface (PDATA, PCLK and PALE).
- Interface to the bi-directional synchronous data signal interface (DIO and DCLK).
- Optionally the microcontroller can do data encoding / decoding.
- Optionally the microcontroller can monitor the frequency lock status from pin CHP_OUT (LOCK).
- Optionally the microcontroller can monitor the RSSI output for signal strength acquisition.

Connecting the microcontroller

The microcontroller uses 3 output pins for the configuration interface (PDATA, PCLK and PALE). PDATA should be a bi-directional pin for data read-back. A bi-directional pin is used for data (DIO) to be transmitted and data received. DCLK providing the data timing should be connected to a microcontroller input. Optionally another pin can be used to monitor the LOCK signal (available at the CHP_OUT pin). This signal is logic level high when the PLL is in lock. See Figure 6.

Also the RSSI signal can be connected to the microcontroller if it has an analogue ADC input.

The microcontroller pins connected to PDATA and PCLK can be used for other purposes when the configuration interface is not used. PDATA and PCLK are high impedance inputs as long as PALE is high.

PALE has an internal pull-up resistor and should be left open (tri-stated by the microcontroller) or set to a high level during power down mode in order to prevent a trickle current flowing in the pull-up. The pin state in power down mode is summarized in Table 3.

Pin	Pin state	Note
PDATA	Input	Should be driven high or low
PCLK	Input	Should be driven high or low
PALE	Input with internal pull-up resistor	Should be driven high or high-impedance to minimize power consumption
DIO	Input	Should be driven high or low
DCLK	High-impedance output	

Table 3. TR1000 pins in power-down mode

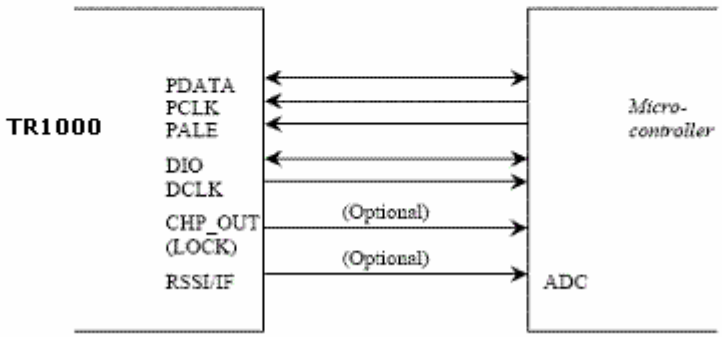


Figure 6. Microcontroller interface

Signal interface

The signal interface consists of DIO and DCLK and is used for the data to be transmitted and data received. DIO is the bi-directional data line and DCLK provides a synchronous clock both during data transmission and data reception.

The **TR1000** can be used with NRZ (Non-Return-to-Zero) data or Manchester (also known as bi-phase-level) encoded data. **TR1000** can also synchronise the data from the demodulator and provide the data clock at DCLK.

TR1000 can be configured for three different data formats:

Synchronous NRZ mode. In transmit mode **TR1000** provides the data clock at DCLK, and DIO is used as data input. Data is clocked into **TR1000** at the rising edge of DCLK. The data is modulated at RF without encoding. **TR1000** can be configured for the data rates 0.6, 1.2, 2.4, 4.8, 9.6, 19.2, 38.4 or 76.8 kbit/s. For 38.4 and 76.8 kbit/s a crystal frequency of 14.7456 MHz must be used. In receive mode **TR1000** does the synchronisation and provides received data clock at DCLK and data at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 7.

Synchronous Manchester encoded mode. In transmit mode **TR1000** provides the data clock at DCLK, and DIO is used as data input. Data is clocked into **TR1000** at the rising edge of DCLK and should be in NRZ format. The data is modulated at RF with Manchester code. The encoding is done by **TR1000**! In this mode **TR1000** can be configured for the data rates 0.3, 0.6, 1.2, 2.4, 4.8, 9.6, 19.2 or 38.4 kbit/s. The 38.4 kbit/s rate corresponds to the maximum 76.8 kBaud due to the Manchester encoding. For 38.4 and 76.8 kBaud a crystal frequency of 14.7456 MHz must be used. In receive mode **TR1000** does the synchronisation and provides received data clock at DCLK and data at DIO. **TR1000** does the decoding and NRZ data is presented at DIO. The data should be clocked into the interfacing circuit at the rising edge of DCLK. See Figure 8.

Transparent Asynchronous UART mode. In transmit mode DIO is used as data input. The data is modulated at RF without synchronisation or encoding. In receive mode the raw data signal from the demodulator is sent to the output. No synchronisation or decoding of the signal is done in **TR1000** and should be done by the interfacing circuit. The DCLK pin is used as data output in this mode. Data rates in the range from 0.6 to 76.8 kBaud can be used. For 38.4 and 76.8 kBaud a crystal frequency of 14.7456 MHz must be used. See Figure 9.

Manchester encoding and decoding

In the *Synchronous Manchester encoded mode* **TR1000** uses Manchester coding when modulating the data. The **TR1000** also performs the data decoding and synchronisation. The Manchester code is based on transitions; a "0" is encoded as a low-to-high transition, a "1" is encoded as a high-to-low transition. See Figure 10.

The **TR1000** can detect a Manchester decoding violation and will set a Manchester Violation Flag when such a violation is detected in the incoming signal. The threshold limit for the Manchester Violation can be set in the *MODEM1* register. The Manchester Violation Flag can be monitored at the CHP_OUT (LOCK) pin, configured in the *LOCK* register.

The Manchester code ensures that the signal has a constant DC component, which is necessary in some FSK demodulators.

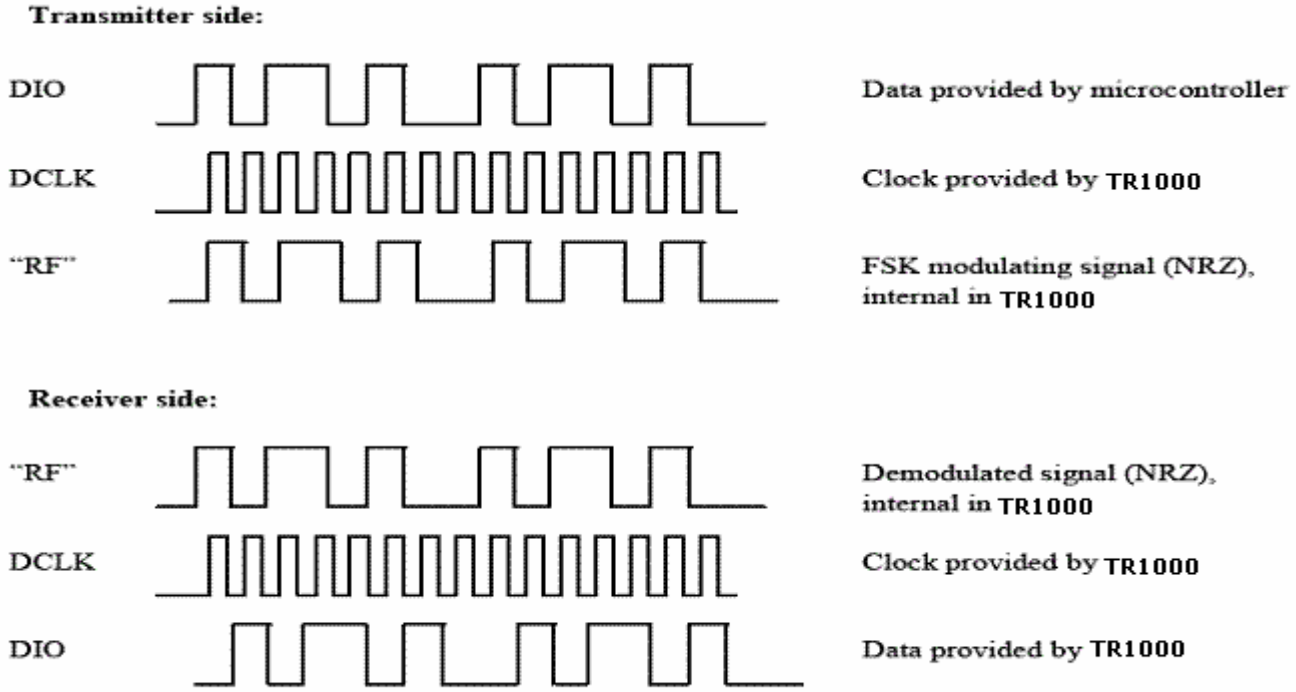


Figure 7. Synchronous NRZ mode

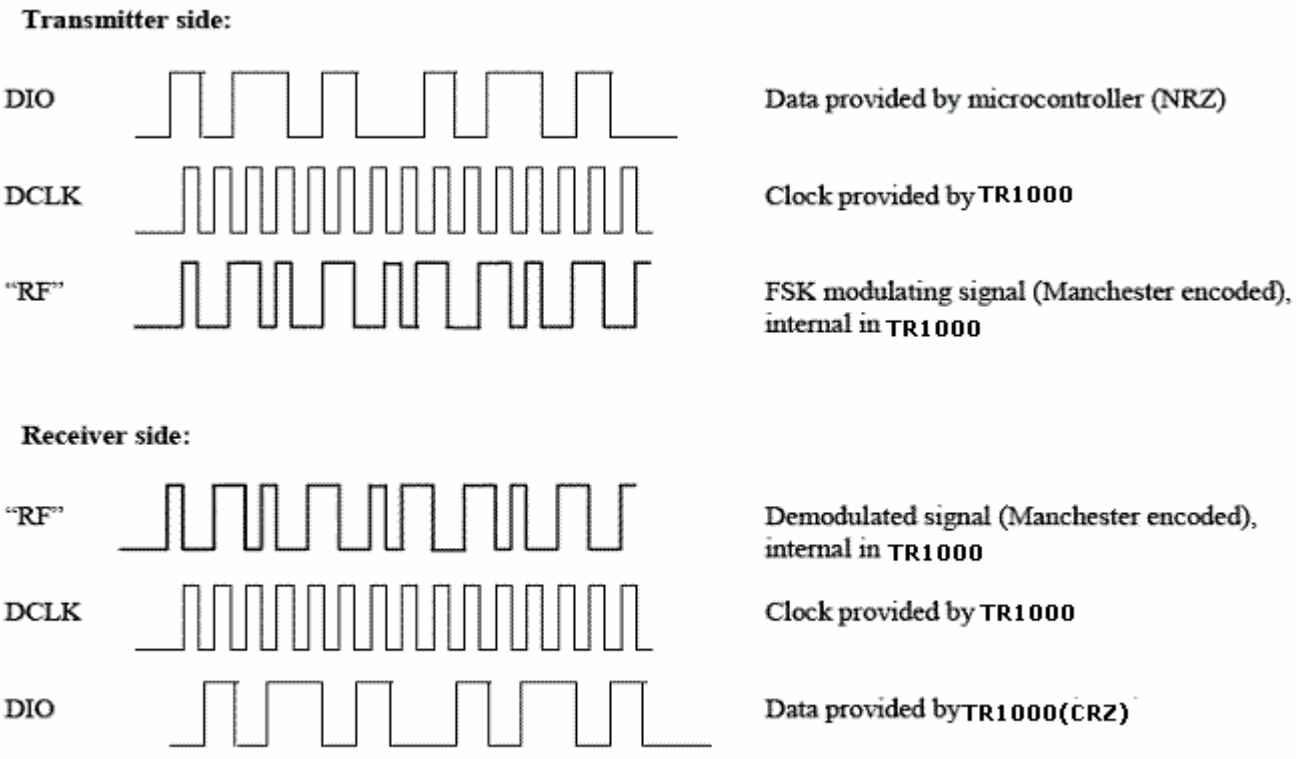
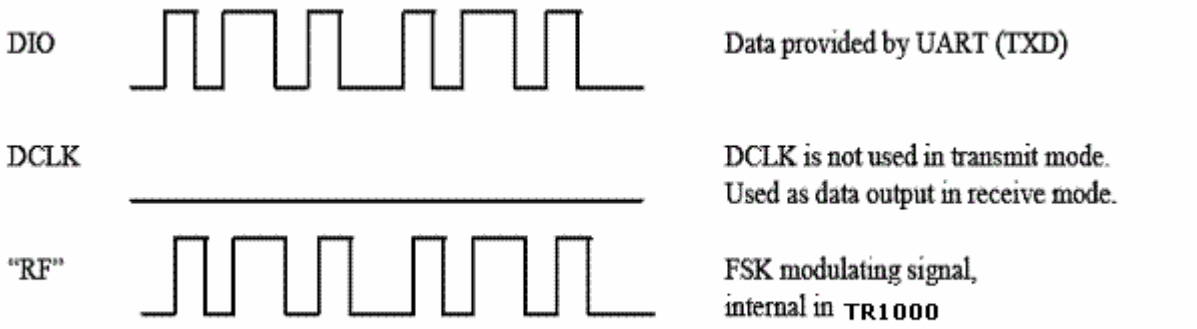


Figure 8. Synchronous Manchester encoded mode

Transmitter side:



Receiver side:

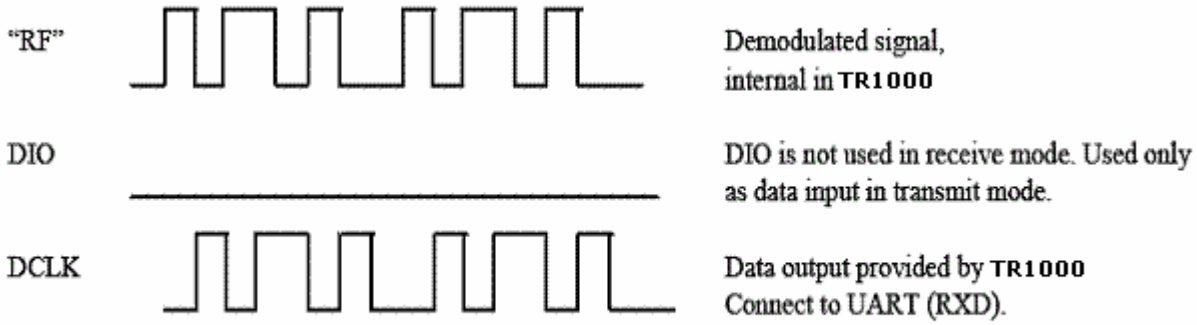


Figure 9. Transparent Asynchronous UART mode

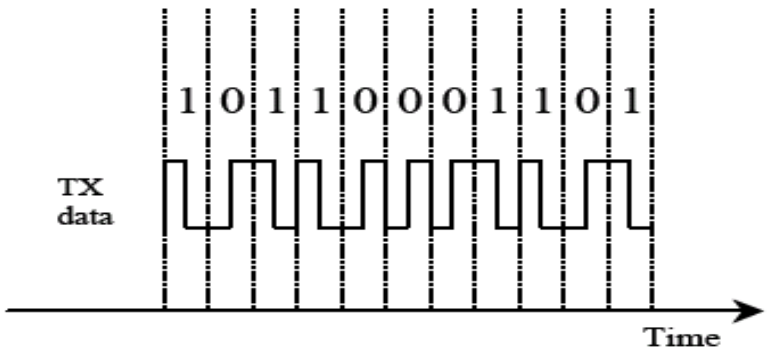


Figure 10. Manchester encoding

Settling MODEM1. SETTLING (1:0)	Manual Lock		Automatic Lock	
	NRZ mode MODEM1.LOCK_ AVG_MODE='1' MODEM1.LOCK_ AVG_IN='0'=→'1'**	UART mode MODEM1.LOCK_ AVG_MODE='1' MODEM1.LOCK_ AVG_IN='0'=→'1'**	NRZ mode MODEM1.LOCK_ AVG_MODE='0' MODEM1.LOCK_ AVG_IN='X'***	UART mode MODEM1.LOCK_ AVG_MODE='0' MODEM1.LOCK_ AVG_IN='X'***
00	14	11	16	16
01	25	22	32	32
10	46	43	64	64
11	89	86	128	128

Notes:
** The averaging filter is locked when **MODEM1.LOCK_AVG_IN** is set to 1
*** X = Do not care. The timer for the automatic lock is started when RX mode is set in the **RFMAIN** register
Also please note that in addition to the number of bits required to lock the filter, you need to add the number of bits needed for the preamble detector. See the next section for more information.

Table 4. Minimum preamble bits for locking the averaging filter, NRZ and UART mode

Settling MODEM1. SETTLING (1:0)	Free-running Manchester mode MODEM1.LOCK_ AVG_MODE='1' MODEM1.LOCK_ AVG_IN='0'
00	23
01	34
10	55
11	98

Table 5. Minimum number preamble chips for averaging filter, Manchester mode

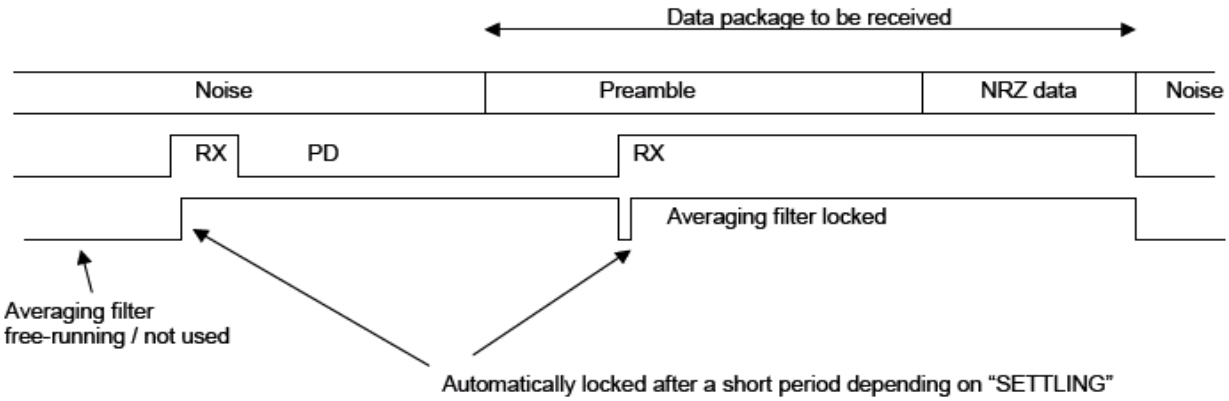


Figure 12. Automatic locking of the averaging filter

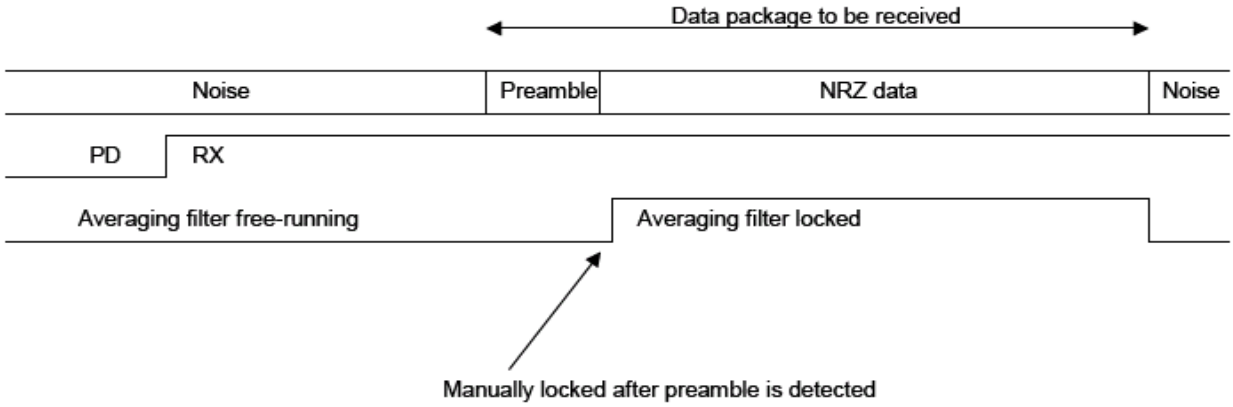


Figure 13. Manual locking of the averaging filter

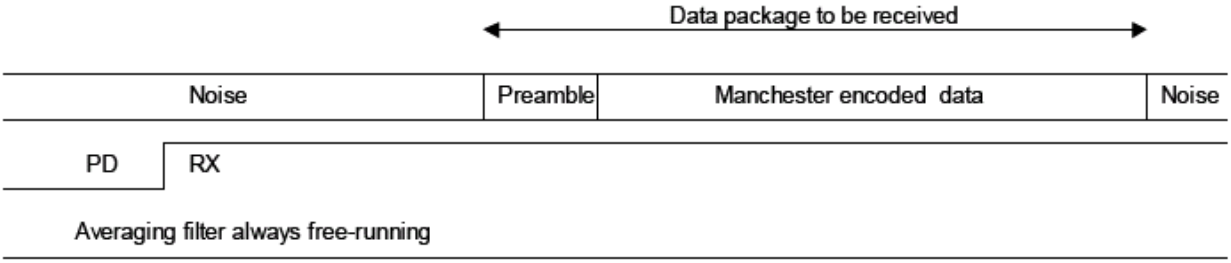


Figure 14. Free-running averaging filter

Receiver sensitivity versus data rate and frequency separation

The receiver sensitivity depends on the data rate, the data format, FSK frequency separation and the RF frequency. Typical figures for the receiver sensitivity (BER = 10^{-3}) are shown in Table 6 for 64 kHz frequency separations and Table 7 for 20 kHz separations. Optimised sensitivity configurations are used. For best performance the frequency separation should be as high as possible especially at high data rates. Table 8 shows the sensitivity for low current settings. See page 28 for how to program different current consumption.

Data rate [kBaud]	Separation [kHz]	433 MHz			868 MHz		
		NRZ mode	Manchester mode	UART mode	NRZ mode	Manchester mode	UART mode
0.6	64	-113	-114	-113	-110	-111	-110
1.2	64	-111	-112	-111	-108	-109	-108
2.4	64	-109	-110	-109	-106	-107	-106
4.8	64	-107	-108	-107	-104	-105	-104
9.6	64	-105	-106	-105	-102	-103	-102
19.2	64	-103	-104	-103	-100	-101	-100
38.4	64	-102	-103	-102	-98	-99	-98
76.8	64	-100	-101	-100	-97	-98	-97
Average current consumption		9.3 mA			11.8 mA		

Table 6. Receiver sensitivity as a function of data rate at 433 and 868 MHz, BER = 10^{-3}, frequency separation 64 kHz, normal current settings

Table 6. Receiver sensitivity as a function of data rate at 433 and 868 MHz, BER = 10^{-3}, frequency separation 64 kHz, normal current settings

Data rate [kBaud]	Separation [kHz]	433 MHz			868 MHz		
		NRZ mode	Manchester mode	UART mode	NRZ mode	Manchester mode	UART mode
0.6	20	-109	-111	-109	-106	-108	-106
1.2	20	-108	-110	-108	-104	-106	-104
2.4	20	-106	-108	-106	-103	-105	-103
4.8	20	-104	-106	-104	-101	-103	-101
9.6	20	-103	-104	-103	-100	-101	-100
19.2	20	-102	-103	-102	-99	-100	-99
38.4	20	-98	-100	-98	-98	-99	-98
76.8	20	-94	-98	-94	-94	-96	-94
Average current consumption		9.3 mA			11.8 mA		

Table 7. Receiver sensitivity as a function of data rate at 433 and 868 MHz, BER = 10^{-3}, frequency separation 20 kHz, normal current settings

Data rate [kBaud]	Separation [kHz]	433 MHz			868 MHz		
		NRZ mode	Manchester mode	UART mode	NRZ mode	Manchester mode	UART mode
0.6	64	-111	-113	-111	-107	-109	-107
1.2	64	-110	-111	-110	-106	-107	-106
2.4	64	-108	-109	-108	-104	-105	-104
4.8	64	-106	-107	-106	-102	-103	-102
9.6	64	-104	-105	-104	-100	-101	-100
19.2	64	-102	-103	-102	-98	-99	-98
38.4	64	-101	-102	-101	-96	-97	-96
76.8	64	-99	-100	-99	-95	-96	-95
Average current consumption		7.4 mA			9.6 mA		

Table 8. Receiver sensitivity as a function of data rate at 433 and 868 MHz, BER = 10^{-3}, frequency separation 64 kHz , low current settings

Frequency programming

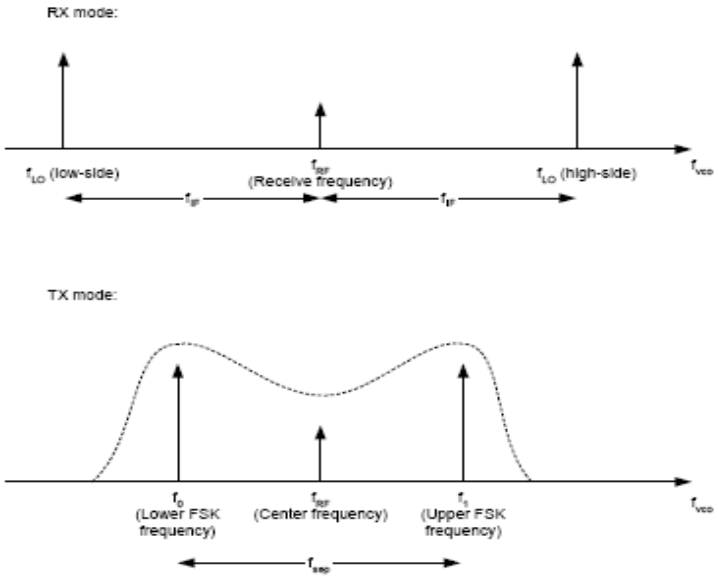


Figure 15. Relation between f_{vco}, f_{if}, and LO frequency

The frequency synthesiser (PLL) is controlled by the frequency word in the configuration registers. There are two frequency words, *A* and *B*, which can be programmed to two different frequencies. One of the frequency words can be used for RX (local oscillator frequency) and the other for TX (transmitting frequency, f_0). This makes it possible to switch very fast between RX mode and TX mode. They can also be used for RX (or TX) on two different channels. The MAIN.F_REG control bit performs selection of frequency word A or B.

The frequency word, *FREQ*, is 24 bits (3 bytes) located in *FREQ_2A:FREQ_1A:FREQ_0A* and *FREQ_2B:FREQ_1B:FREQ_0B* for the *A* and *B* word, respectively.

The frequency word *FREQ* can be calculated from:

$$f_{VCO} = f_{ref} \cdot \frac{FREQ + FSEP \cdot TXDATA + 8192}{16384},$$

where *TXDATA* is 0 or 1 in transmit mode depending on the data bit to be transmitted on DIO. In receive mode *TXDATA* is always 0.

The reference frequency f_{ref} is the crystal oscillator clock divided by *PLL.REFDIV*, a number between 2 and 14 that should be chosen such that:

$$1.0 \text{ MHz} \le f_{ref} \le 2.46 \text{ MHz}$$

Thus, the reference frequency f_{ref} is:

$$f_{ref} = \frac{f_{xosc}}{REFDIV}$$

f_{VCO} is the Local Oscillator (LO) frequency in receive mode, and the f_0 frequency in transmit mode (lower FSK frequency). The LO frequency must be $f_{RF} - f_{IF}$ or $f_{RF} + f_{IF}$ giving low-side or high side LO injection respectively. Note that the data on DIO will be inverted if high-side LO is used.

The upper FSK transmit frequency is given by:

$$f_1 = f_0 + f_{sep},$$

where the frequency separation f_{sep} is set by the 11 bit separation word (*FSEP1:FSEP0*):

$$f_{sep} = f_{ref} \cdot \frac{FSEP}{16384}$$

Clearing *PLL.ALARM_DISABLE* will enable generation of the frequency alarm bits *PLL.ALARM_H* and *PLL.ALARM_L*. These bits indicate that the frequency synthesis PLL is near the limit of generate the frequency requested, and the PLL should be recalibrated.

It is recommended that the *LOCK_CONTINOUS* bit in the LOCK register is checked when changing frequencies and when changing between RX and TX mode. If lock is not achieved, a calibration should be performed.

Recommended RX settings for ISM frequencies

Shown in Table 9 are the recommended RX frequency synthesiser settings for a few operating frequencies in the popular ISM bands. These settings ensure optimum configuration of the synthesiser in receive mode for best sensitivity. For some settings of the synthesiser (combinations of RF frequencies and reference frequency), the receiver sensitivity is degraded. The FSK frequency separation is set to 64 kHz. The SmartRF® Studio can be used to generate optimised configuration data as well. Also an application note (AN011) and a spreadsheet are available from Chipcon generating configuration data for any frequency giving optimum sensitivity.

ISM Frequency [MHz]	Actual frequency [MHz]	Crystal frequency [MHz]	Low-side / high- side LO*	Reference divider REFDIV (decimal)	Frequency word RX mode FREQ (decimal)	Frequency word RX mode FREQ (hex)
315	315.037200	3.6864	High-side	3	4194304	400000
		7.3728		6	4194304	400000
		11.0592		9	4194304	400000
		14.7456		12	4194304	400000
433.3	433.302000	3.6864	Low-side	3	5775168	580000
		7.3728		6	5775168	580000
		11.0592		9	5775168	580000
		14.7456		12	5775168	580000
433.9	433.916400	3.6864	Low-side	3	5775360	582000
		7.3728		6	5775360	582000
		11.0592		9	5775360	582000
		14.7456		12	5775360	582000
434.5	434.530800	3.6864	Low-side	3	5783552	584000
		7.3728		6	5783552	584000
		11.0592		9	5783552	584000
		14.7456		12	5783552	584000
868.3	868.297200	3.6864	Low-side	2	7708672	75A000
		7.3728		4	7708672	75A000
		11.0592		6	7708672	75A000
		14.7456		8	7708672	75A000
868.95	868.918800	3.6864	High-side	2	7716864	75C000
		7.3728		4	7716864	75C000
		11.0592		6	7716864	75C000
		14.7456			7716864	75C000
869.525	869.526000	3.6864	Low-side	3	11583488	B0C000
		7.3728		6	11583488	B0C000
		11.0592		9	11583488	B0C000
		14.7456		12	11583488	B0C000
869.85	869.840400	3.6864	High-side	2	7725056	75E000
		7.3728		4	7725056	75E000
		11.0592		6	7725056	75E000
		14.7456		8	7725056	75E000
915	914.998800	3.6864	High-side	2	8126464	7C0000
		7.3728		4	8126464	7C0000
		11.0592		6	8126464	7C0000
		14.7456		8	8126464	7C0000

*Note: When using high-side LO injection the data at DIO will be inverted.

Table 9. Recommended settings for ISM frequencies

Output power programming

The RF output power is programmable and controlled by the PA_POW register. Table 11 shows the closest programmable value for output powers in steps of 1 dB. The typical current consumption is also shown.

In power down mode the PA_POW should be set to 00h for minimum leakage current.

Output power [dBm]	RF frequency 433 MHz		RF frequency 868 MHz	
	PA_POW [hex]	Current consumption, typ. [mA]	PA_POW [hex]	Current consumption, typ. [mA]
-20	01	5.3	02	8.6
-19	01	6.9	02	8.8
-18	02	7.1	03	9.0
-17	02	7.1	03	9.0
-16	02	7.1	04	9.1
-15	03	7.4	05	9.3
-14	03	7.4	05	9.3
-13	03	7.4	06	9.5
-12	04	7.6	07	9.7
-11	04	7.6	08	9.9
-10	05	7.9	09	10.1
-9	05	7.9	0B	10.4
-8	06	8.2	0C	10.6
-7	07	8.4	0D	10.8
-6	08	8.7	0F	11.1
-5	09	8.9	40	13.8
-4	0A	9.6	50	14.5
-3	0B	9.4	50	14.5
-2	0C	9.7	60	15.1
-1	0E	10.2	70	15.8
0	0F	10.4	80	16.8
1	40	11.8	90	17.2
2	50	12.8	B0	18.5
3	50	12.8	C0	19.2
4	60	13.8	F0	21.3
5	70	14.8	FF	25.4
6	80	15.8		
7	90	16.8		
8	C0	20.0		
9	E0	22.1		
10	FF	26.7		

Table 11. Output power settings and typical current consumption

Configuration registers

The configuration of TR1000 is done by programming 22 8-bit configuration registers. The configuration data based on selected system parameters are most easily found by using the SmartRF® Studio software. A complete description of the registers are given in the following tables. After a RESET is programmed all the registers have default values.

REGISTER OVERVIEW

ADDRESS	Byte Name	Description
00h	MAIN	MAIN Register
01h	FREQ_2A	Frequency Register 2A
02h	FREQ_1A	Frequency Register 1A
03h	FREQ_0A	Frequency Register 0A
04h	FREQ_2B	Frequency Register 2B
05h	FREQ_1B	Frequency Register 1B
06h	FREQ_0B	Frequency Register 0B
07h	FSEP1	Frequency Separation Register 1
08h	FSEP0	Frequency Separation Register 0
09h	CURRENT	Current Consumption Control Register
0Ah	FRONT_END	Front End Control Register
0Bh	PA_POW	PA Output Power Control Register
0Ch	PLL	PLL Control Register
0Dh	LOCK	LOCK Status Register and signal select to CHP_OUT (LOCK) pin
0Eh	CAL	VCO Calibration Control and Status Register
0Fh	MODEM2	Modem Control Register 2
10h	MODEM1	Modem Control Register 1
11h	MODEM0	Modem Control Register 0
12h	MATCH	Match Capacitor Array Control Register for RX and TX impedance matching
13h	FSCTRL	Frequency Synthesiser Control Register
14h		Reserved
15h		Reserved
16h		Reserved
17h		Reserved
18h		Reserved
19h		Reserved
1Ah		Reserved
1Bh		Reserved
1Ch	PRESCALER	Prescaler and IF-strip test control register
40h	TEST6	Test register for PLL LOOP
41h	TEST5	Test register for PLL LOOP
42h	TEST4	Test register for PLL LOOP (must be updated as specified)
43h	TEST3	Test register for VCO
44h	TEST2	Test register for Calibration
45h	TEST1	Test register for Calibration
46h	TEST0	Test register for Calibration

MAIN Register (00h)

REGISTER	NAME	Default value	Active	Description
MAIN[7]	RXTX	-	-	RX/TX switch, 0 : RX , 1 : TX
MAIN[6]	F_REG	-	-	Selection of Frequency Register, 0 : Register A, 1 : Register B
MAIN[5]	RX_PD	-	H	Power Down of LNA, Mixer, IF, Demodulator, RX part of Signal Interface
MAIN[4]	TX_PD	-	H	Power Down of TX part of Signal Interface, PA
MAIN[3]	FS_PD	-	H	Power Down of Frequency Synthesiser
MAIN[2]	CORE_PD	-	H	Power Down of Crystal Oscillator Core
MAIN[1]	BIAS_PD	-	H	Power Down of BIAS (Global_Current_Generator) and Crystal Oscillator Buffer
MAIN[0]	RESET_N	-	L	Reset, active low. Writing RESET_N low will write default values to all other registers than MAIN. Bits in MAIN do not have a default value, and will be written directly through the configurations interface. Must be set high to complete reset.

FREQ_2A Register (01h)

REGISTER	NAME	Default value	Active	Description
FREQ_2A[7:0]	FREQ_A[23:16]	01110101	-	8 MSB of frequency control word A

FREQ_1A Register (02h)

REGISTER	NAME	Default value	Active	Description
FREQ_1A[7:0]	FREQ_A[15:8]	10100000	-	Bit 15 to 8 of frequency control word A

FREQ_0A Register (03h)

REGISTER	NAME	Default value	Active	Description
FREQ_0A[7:0]	FREQ_A[7:0]	11001011	-	8 LSB of frequency control word A

FREQ_2B Register (04h)

REGISTER	NAME	Default value	Active	Description
FREQ_2B[7:0]	FREQ_B[23:16]	01110101	-	8 MSB of frequency control word B

FREQ_1B Register (05h)

REGISTER	NAME	Default value	Active	Description
FREQ_1B[7:0]	FREQ_B[15:8]	10100101	-	Bit 15 to 8 of frequency control word B

FREQ_0B Register (06h)

REGISTER	NAME	Default value	Active	Description
FREQ_0B[7:0]	FREQ_B[7:0]	01001110	-	8 LSB of frequency control word B

FSEP1 Register (07h)

REGISTER	NAME	Default value	Active	Description
FSEP1[7:3]	-	-	-	Not used
FSEP1[2:0]	FSEP_MSB[2:0]	000	-	3 MSB of frequency separation control

FSEP0 Register (08h)

REGISTER	NAME	Default value	Active	Description
FSEP0[7:0]	FSEP_LSB[7:0]	01011001	-	8 LSB of frequency separation control

CURRENT Register (09h)

REGISTER	NAME	Default value	Active	Description
CURRENT[7:4]	VCO_CURRENT[3:0]	1100	-	Control of current in VCO core for TX and RX 0000 : 150µA 0001 : 250µA 0010 : 350µA 0011 : 450µA 0100 : 950µA, use for RX, f= 400 - 500 MHz 0101 : 1050µA 0110 : 1150µA 0111 : 1250µA 1000 : 1450µA, use for RX, f<400 MHz and f>500 MHz; and TX, f= 400 - 500 MHz 1001 : 1550µA, use for TX, f<400 MHz 1010 : 1650µA 1011 : 1750µA 1100 : 2250µA 1101 : 2350µA 1110 : 2450µA 1111 : 2550µA, use for TX, f>500 MHz
CURRENT[3:2]	LO_DRIVE[1:0]	10		Control of current in VCO buffer for LO drive 00 : 0.5mA, use for TX 01 : 1.0mA , use for RX, f<500 MHz* 10 : 1.5mA, 11 : 2.0mA, use for RX, f>500 MHz * * LO_DRIVE can be reduced to save current in RX mode. See Table 10 for details
CURRENT[1:0]	PA_DRIVE[1:0]	10		Control of current in VCO buffer for PA 00 : 1mA, use for RX 01 : 2mA, use for TX, f<500 MHz 10 : 3mA 11 : 4mA, use for TX, f>500 MHz

FRONT_END Register (0Ah)

REGISTER	NAME	Default value	Active	Description
FRONT_END[7:6]	-	00	-	Not used
FRONT_END[5]	BUF_CURRENT	0	-	Control of current in the LNA_FOLLOWER 0 : 520uA, use for f<500 MHz 1 : 690uA, use for f>500 MHz * *BUF_CURRENT can be reduced to save current in RX mode. See Table 10 for details.
FRONT_END[4:3]	LNA_CURRENT [1:0]	01	-	Control of current in LNA 00 : 0.8mA, use for f<500 MHz * 01 : 1.4mA 10 : 1.8mA, use for f>500 MHz * 11 : 2.2mA *LNA_CURRENT can be reduced to save current in RX mode. See Table 10 for details.
FRONT_END[2:1]	IF_RSSI[1:0]	00	-	Control of IF_RSSI pin 00 : Internal IF and demodulator, RSSI inactive 01 : RSSI active, RSSI/IF is analog RSSI output 10 : External IF and demodulator, RSSI/IF is mixer output. Internal IF in power down mode. 11 : Not used
FRONT_END[0]	XOSC_BYPASS	0	-	0 : Internal XOSC enabled 1 : Power-Down of XOSC, external CLK used

PA_POW Register (0Bh)

REGISTER	NAME	Default value	Active	Description
PA_POW[7:4]	PA_HIGHPOWER[3:0]	0000	-	Control of output power in high power array. Should be 0000 in PD mode . See Table 11 page 32 for details.
PA_POW[3:0]	PA_LOWPOWER[3:0]	1111	-	Control of output power in low power array Should be 0000 in PD mode. See Table 11 page 32 for details.

PLL Register (0Ch)

REGISTER	NAME	Default value	Active	Description
PLL[7]	EXT_FILTER	0	-	1 : External loop filter 0 : Internal loop filter 1-to-0 transition samples F_COMP comparator when BREAK_LOOP=1 (TEST3)
PLL[6:3]	REFDIV[3:0]	0010	-	Reference divider 0000 : Not allowed 0001 : Not allowed 0010 : Divide by 2 0011 : Divide by 3 ..... 1111 : Divide by 15
PLL[2]	ALARM_DISABLE	0	h	0 : Alarm function enabled 1 : Alarm function disabled
PLL[1]	ALARM_H	-	-	Status bit for tuning voltage out of range (too close to VDD)
PLL[0]	ALARM_L	-	-	Status bit for tuning voltage out of range (too close to GND)

LOCK Register (0Dh)

REGISTER	NAME	Default value	Active	Description
LOCK[7:4]	LOCK_SELECT[3:0]	0000	-	Selection of signals to CHP_OUT (LOCK) pin 0000 : Normal, pin can be used as CHP_OUT 0001 : LOCK_CONTINUOUS (active high) 0010 : LOCK_INSTANT (active high) 0011 : ALARM_H (active high) 0100 : ALARM_L (active high) 0101 : CAL_COMPLETE (active high) 0110 : IF_OUT 0111 : REFERENCE_DIVIDER Output 1000 : TX_PDB (active high, activates external PA when TX_PD=0) 1001 : Manchester Violation (active high) 1010 : RX_PDB (active high, activates external LNA when RX_PD=0) 1011 : Not defined 1100 : Not defined 1101 : LOCK_AVG_FILTER 1110 : N_DIVIDER Output 1111 : F_COMP
LOCK[3]	PLL_LOCK_ ACCURACY	0	-	0 : Sets Lock Threshold = 127, Reset Lock Threshold = 111. Corresponds to a worst case accuracy of 0.7% 1 : Sets Lock Threshold = 31, Reset Lock Threshold =15. Corresponds to a worst case accuracy of 2.8%
LOCK[2]	PLL_LOCK_ LENGTH	0	-	0 : Normal PLL lock window 1 : Not used
LOCK[1]	LOCK_INSTANT	-	-	Status bit from Lock Detector
LOCK[0]	LOCK_CONTINUOUS	-	-	Status bit from Lock Detector

CAL Register (0Eh)

REGISTER	NAME	Default value	Active	Description
CAL[7]	CAL_START	0	↑	↑ 1 : Calibration started 0 : Calibration inactive CAL_START must be set to 0 after calibration is done
CAL[6]	CAL_DUAL	0	H	1 : Store calibration in both A and B 0 : Store calibration in A or B defined by MAIN[6]
CAL[5]	CAL_WAIT	0	H	1 : Normal Calibration Wait Time 0 : Half Calibration Wait Time The calibration time is proportional to the internal reference frequency. 2 MHz reference frequency gives 14 ms wait time.
CAL[4]	CAL_CURRENT	0	H	1 : Calibration Current Doubled 0 : Normal Calibration Current
CAL[3]	CAL_COMPLETE	0	H	Status bit defining that calibration is complete
CAL[2:0]	CAL_ITERATE	101	H	Iteration start value for calibration DAC 000 - 101: Not used 110 : Normal start value 111 : Not used

MODEM2 Register (0Fh)

REGISTER	NAME	Default value	Active	Description
MODEM2[7]	PEAKDETECT	1	H	Peak Detector and Remover disabled or enabled 0 : Peak detector and remover is disabled 1 : Peak detector and remover is enabled
MODEM2[6:0]	PEAK_LEVEL_OFFSET[6:0]	0010110	-	Threshold level for Peak Remover in Demodulator. Correlated to frequency deviation, see note.

Note: PEAK_LEVEL_OFFSET[6:0] = $\frac{Fs}{IF_{low}} - \frac{Fs}{IF_{low} + \Delta f/2} \cdot \frac{5}{8}$ where $Fs = \frac{f\_xosc}{XOSC\_FREQ + 1}$

and $IF_{low} = 150kHz - 2 \bullet f\_rf \bullet XTAL\_accuracy$ and Δf is the separation

MODEM1 Register (10h)

REGISTER	NAME	Default value	Active	Description
MODEM1[7:5]	MLIMIT	011	-	Sets the limit for the Manchester Violation Flag. A Manchester Value = 14 is a perfect bit and a Manchester Value = 0 is a constant level (an unbalanced corrupted bit) 000 : No Violation Flag is set 001 : Violation Flag is set for Manchester Value < 1 010 : Violation Flag is set for Manchester Value < 2 011 : Violation Flag is set for Manchester Value < 3 100 : Violation Flag is set for Manchester Value < 4 101 : Violation Flag is set for Manchester Value < 5 110 : Violation Flag is set for Manchester Value < 6 111 : Violation Flag is set for Manchester Value < 7
MODEM1[4]	LOCK_AVG_IN	0	H	Lock control bit of Average Filter 0 : Average Filter is free-running 1 : Average Filter is locked
MODEM1[3]	LOCK_AVG_MODE	0	-	Automatic lock of Average Filter 0 : Lock of Average Filter is controlled automatically 1 : Lock of Average Filter is controlled by LOCK_AVG_IN
MODEM1[2:1]	SETTLING[1:0]	11	-	Settling Time of Average Filter 00 : 11 baud settling time, worst case 1.2dB loss in sensitivity 01 : 22 baud settling time, worst case 0.6dB loss in sensitivity 10 : 43 baud settling time, worst case 0.3dB loss in sensitivity 11 : 86 baud settling time, worst case 0.15dB loss in sensitivity
MODEM1[0]	MODEM_RESET_N	1	L	Separate reset of MODEM

MODEM0 Register (11h)

REGISTER	NAME	Default value	Active	Description
MODEM0[7]	-	-	-	Not used
MODEM0[6:4]	BAUDRATE[2:0]	010	-	000 : 0.6 kBaud 001 : 1.2 kBaud 010 : 2.4 kBaud 011 : 4.8 kBaud 100 : 9.6 kBaud 101 : 19.2, 38.4 and 76.8 kBaud 110 : Not used 111 : Not used
MODEM0[3:2]	DATA_FORMAT[1:0]	01	-	00 : NRZ operation. 01 : Manchester operation 10 : Transparent Asyncronous UART operation 11 : Not used
MODEM0[1:0]	XOSC_FREQ[1:0]	00	-	Selection of XTAL frequency range 00 : 3MHz - 4MHz crystal, 3.6864MHz recommended Also used for 76.8 kBaud, 14.7456MHz 01 : 6MHz - 8MHz crystal, 7.3728MHz recommended Also used for 38.4 kBaud, 14.7456MHz 10 : 9MHz - 12MHz crystal, 11.0592 MHz recommended 11 : 12MHz - 16MHz crystal, 14.7456MHz recommended

MATCH Register (12h)

REGISTER	NAME	Default value	Active	Description
MATCH[7:4]	RX_MATCH[3:0]	0000	-	Selects matching capacitor array value for RX, step size is 0.4 pF 0001: Use for RF frequency > 500 MHz 0111: Use for RF frequency < 500 MHz
MATCH[3:0]	TX_MATCH[3:0]	0000	-	Selects matching capacitor array value for TX, step size is 0.4 pF

FSCTRL Register (13h)

REGISTER	NAME	Default value	Active	Description
FSCTRL[7:4]	-	-	-	Not used
FSCTRL[3:1]				Reserved
FSCTRL[0]	FS_RESET_N	1	L	Separate reset of frequency synthesizer

PRESCALER Register (1Ch)

REGISTER	NAME	Default value	Active	Description
PRESCALER[7:6]	PRE_SWING[1:0]	00	-	Prescaler swing. Fractions for PRE_CURRENT[1:0] = 00 00 : 1 * Nominal Swing 01 : 2/3 * Nominal Swing 10 : 7/3 * Nominal Swing 11 : 5/3 * Nominal Swing
PRESCALER[5:4]	PRE_CURRENT [1:0]	00	-	Prescaler current scaling 00 : 1 * Nominal Current 01 : 2/3 * Nominal Current 10 : 1/2 * Nominal Current 11 : 2/5 * Nominal Current
PRESCALER[3]	IF_INPUT	0	-	0 : Nominal setting 1 : RSSI/IF pin is input to IF-strips
PRESCALER[2]	IF_FRONT	0	-	0 : Nominal setting 1 : Output of IF_Front_amp is switched to RSSI/IF pin
PRESCALER[1:0]	-	00	-	Not used

TEST6 Register (for test only, 40h)

REGISTER	NAME	Default value	Active	Description
TEST6[7]	LOOPFILTER_TP1	0	-	1 : Select testpoint 1 to CHP_OUT 0 : CHP_OUT tied to GND
TEST6 [6]	LOOPFILTER_TP2	0	-	1 : Select testpoint 2 to CHP_OUT 0 : CHP_OUT tied to GND
TEST6 [5]	CHP_OVERRIDE	0	-	1 : use CHP_CO[4:0] value 0 : use calibrated value
TEST6[4:0]	CHP_CO[4:0]	10000	-	Charge_Pump Current DAC override value

TEST5 Register (for test only, 41h)

REGISTER	NAME	Default value	Active	Description
TEST5[7:6]	-	-	-	Not used
TEST5[5]	CHP_DISABLE	0	-	1 : CHP up and down pulses disabled 0 : normal operation
TEST5[4]	VCO_OVERRIDE	0	-	1 : use VCO_AO[2:0] value 0 : use calibrated value
TEST5[3:0]	VCO_AO[3:0]	1000	-	VCO_ARRAY override value

TEST4 Register (for test only, 42h)

REGISTER	NAME	Default value	Active	Description
TEST4[7:6]	-	-	-	Not used
TEST4[5:0]	L2KIO[5:0]	100101	h	Constant setting charge pump current scaling/rounding factor. Sets Bandwidth of PLL. Use 3Fh for 9.6 kBaud and higher

TEST3 Register (for test only, 43h)

REGISTER	NAME	Default value	Active	Description
TEST3[7:5]	-	-	-	Not used
TEST3[4]	BREAK_LOOP	0	-	1 : PLL loop open 0 : PLL loop closed
TEST3[3:0]	CAL_DAC_OPEN	0100	-	Calibration DAC override value, active when BREAK_LOOP =1

TEST2 Register (for test only, 44h)

REGISTER	NAME	Default value	Active	Description
TEST2[7:5]	-	-	-	Not used
TEST2[4:0]	CHP_CURRENT [4:0]	-	-	Status vector defining applied CHP_CURRENT value

TEST1 Register (for test only, 45h)

REGISTER	NAME	Default value	Active	Description
TEST1[7:4]	-	-	-	Not used
TEST1[3:0]	CAL_DAC[3:0]	-	-	Status vector defining applied Calibration DAC value

TEST0 Register (for test only, 46h)

REGISTER	NAME	Default value	Active	Description
TEST0[7:4]	-	-	-	Not used
TEST0[3:0]	VCO_ARRAY[3:0]	-	-	Status vector defining applied VCO_ARRAY value